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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,850	DEMPSEY, DENNIS A.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,12-17,19-21 and 23-44* is/are rejected.

7)☒ Claim(s) *7,9-11,18 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/24/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s).(PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 12-14, 26, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., Patent No. 6,329,863, in view of Bradley et al., Patent No. 6,550,664.

With respect to claim 1, Lee teaches an integrated circuit [Fig. 1, semiconductor device 1] having at least one external connection pin [Fig. 1, 50], the pin being coupled to a pad cell [Fig. 1, 110, 210] adapted to provide a signal path from circuitry external to the integrated circuit via the pin to components of the integrated circuit [Fig. 1, 120, 220], and wherein the pad cell includes a first signal path [Fig. 1, 10] being operational under a first set of normal operating conditions and a second signal path [Fig. 1, 20], the second signal path being non-operable under the first set of normal operating conditions [Col. 3, lines 55-67, Col. 4, lines 8-12] and operable on application of a pre-defined signal to the pin, the operation of the second signal path being parallel to and simultaneous with the operation of the first signal path as disclosed in Fig. 1. However, Lee

does not disclose that the pad cell includes a first signal path and a second signal path.

Bradley teaches acoustic resonator filters in microwave packages. Bradley teaches a pad cell [Fig. 4, 12] adapted to provide a signal path from the circuitry external to the integrated circuit, wherein the pad cell [Fig. 4, 12] includes a first signal path [Fig. 4, 19] and a second signal path [Fig. 4, 20].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bradley, which teaches two signal paths on the same pad cell, with the circuit of Lee, for the benefit of reducing the number of bonding pads required per pin, which reduces circuit board manufacturing costs.

With respect to claim 12, Lee teaches that the second signal path may be replicated such that the pad cell provides multiple signal paths that may be operable simultaneously with and in parallel to the first signal path as disclosed in Fig. 3, Col. 5, lines 42-49.

With respect to claim 13, Lee teaches that each o the multiple signal paths [Fig. 1, 10, 20] of the pad cell are individually operable such that at any one time only one signal path of the multiple signal paths is operable [Col. 3, lines 55-67, Col. 4, lines 8-12].

With respect to claim 14, Lee teaches that the pre-defined signal is a signal of larger magnitude than the first set of normal operating conditions [As

shown in Fig. 1, the signal on the first path could be smaller than the signal on the second path and still operate the input circuit 100 satisfactorily].

With respect to claim 26, Lee teaches an integrated circuit [Fig. 1, semiconductor device 1] comprising internal circuitry [Fig. 1, 120, 220], at least one external connection [Fig. 1, 50], a pad cell [Fig. 1, 110, 210] electrically interposed between an external connection and the internal circuitry, the pad cell comprising a first group of components [Fig. 1, 100] adapted to protect the internal circuitry [Fig. 1, 120] from transients at the external connection [Col. 3, lines 23-34] and providing, during normal operating conditions of the integrated circuits, a first signal path to the internal circuitry, a second group of components [Fig. 1, 200] providing a second signal path from the external connection to the internal circuitry and wherein the second signal path is non-operable during the normal operating conditions [Col. 3, lines 55-67, Col. 4, lines 8-12] but on application of a predefined voltage at the external connection becomes operable, the first and second signal paths [Fig. 1, 10, 20] being simultaneously operable.

With respect to claims 31-33, it is well known to use filters for smoothing signals before they are inputted into an internal circuitry. Additionally, there is no significant distinction between analog and digital filter.

2. Claims 2-3 and 34-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., in view of Bradley et al., Patent No. 6,550,664, and further in view of Ohnakado, Publication No. 2002/0033504.

Lee teaches a second signal path, but does not disclose that the second path includes a MOS transistor device, the source and well of the device being coupled to one another. With respect to claim 2, Ohnakado teaches a second signal path that includes a MOS transistor [Fig. 2, transistor 32] device, the source and well of the device being coupled to one another as disclosed in Fig. 2.

Both teachings are analogous semiconductor devices having protective circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ohnakado, which teaches a MOS transistor device having its source and well coupled to one another, with the semiconductor device of Lee for the benefit of forming path for flowing /dispersing large current when a surge due to ESD is impressed from the I/O pad.

With respect to claim 3, Ohnakado teaches that the source and well are coupled to the pin [Fig. 2, at VDD].

With respect to claim 34, Lee teaches an integrated circuit [Fig. 1, semiconductor device 1] comprising internal circuitry [Fig. 1, 120, 220], at least one external connection [Fig. 1, 50], a pad cell [Fig. 1, 110, 210] electrically interposed between an external connection and the internal circuitry, the pad cell comprising a first group of components [Fig. 1, 100] providing, during normal operating conditions of the integrated circuit, a first signal path to the internal circuitry, a second group of components [Fig. 1, 200] providing a second signal

path from the external connection to the internal circuitry and wherein the second signal path is non-operable during the normal operating conditions [Col. 3, lines 55-67, Col. 4, lines 8-12] but on application of a predefined voltage at the external connection becomes operable. However, Lee does not disclose that the second group of components includes a MOS device having the source and well coupled together, the application of the predefined voltage turning the MOS device on and enabling the second signal path.

Ohnakado teaches a second signal path that includes a MOS transistor [Fig. 2, transistor 32] device having the source and well coupled together, the application of the predefined voltage turning the MOS device on and enabling the second signal path [Page 1, paragraph 6, lines 16-20].

With respect to claim 35, Lee teaches that the pad cell further includes circuit components [Fig. 1, 130] adapted to protect the internal circuitry from transients at the external connection [Fig. 1, 50, Col. 3, lines 23-34].

With respect to claim 36, Lee teaches that the circuit components [Fig. 1, 130, 230] adapted to protect the internal circuitry from transients at the external connection [Fig. 1, 50] are provided in one or other of the first and second signal paths [Col. 3, lines 23-26, Col. 4, lines 13-17].

With respect to claim 37, Lee teaches that the circuit components [Fig. 1, 130] adapted to protect the internal circuitry from transients at the external connection [Fig. 1, 50] are provided in the first signal path [Fig. 1, 10, Col. 3, lines 23-26].

With respect to claim 38, Lee teaches that the circuits is configured such that during operation of the second signal path [Fig. 1, 20], the first signal path [Fig. 1, 10] is not operable [Col. 3, lines 55-67, Col. 4, lines 8-12].

With respect to claim 39, Lee teaches that the first signal path [Fig. 1, 10] is available for operation but is not operable [Col. 3, lines 61-67].

With respect to claim 40, Lee teaches that the first signal path [Fig. 1, 10] is disabled [Col. 3, lines 61-67].

With respect to claim 41, Lee teaches that the second signal path includes components [Fig. 1, 240], which may be configured to disable the second signal path [Col. 4, lines 8-12].

With respect to claim 42, Lee teaches that the second signal path may be permanently disabled [Fig. 1, Col. 4, lines 8-12, when fuse 240 is cut, the second protective element 230 does not operate, and therefore permanently disabled].

With respect to claim 43, Lee teaches that the circuit further includes components [Fig. 1, 240], which may be configured to disable the second signal path during the application of the predetermined voltage at the external connection [Fig. 1, 50].

With respect to claim 44, Lee teaches that the second signal path may be permanently disabled [Fig. 1, Col. 4, lines 8-12, when fuse 240 is cut, the second protective element 230 does not operate, and therefore permanently disabled].

3. Claims 4-6, 8, 15-17, 19, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., in view of Bradley and Ohnakado as applied

to claims 2-3 above, and further in view of Schultz et al., Patent No. 5,164,659. Lee and Ohnakado do not teach that the second signal path additionally includes comparator circuitry. With respect to claim 4, Schultz teaches a switching circuit, the circuit comprises a second signal path that additionally includes comparator circuitry [Fig. 1, 32].

All three teachings are analogous MOS switching devices. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Schultz, which teaches a comparator circuitry, with the semiconductor circuit of Lee modified by Ohnakado, for the purpose of detecting and sending a signal indicating the open or close state of the switching MOS device.

With respect to claims 5 and 6, it is notoriously well known in the art that comparator circuitry includes digital gate and analog amplifier.

With respect to claim 8, Schultz teaches that the comparator circuitry [Fig. 1, 32] is coupled in series to a first MOS device [Fig. 1, 24].

With respect to claim 15, Schultz teaches that the comparator circuitry [Fig. 1, 32] includes a first input coupled to the MOS device [Fig. 1, 24], a second input [Fig. 1, Vr] adapted to provide a signal with which the signal coupled from the MOS device is compared with and an output, the output depending on the comparison effected between the first and second inputs.

With respect to claim 16, Schultz teaches that the comparator circuitry [Fig. 1, 32] is configured as a current comparator [the current and voltage are both simultaneously sensed by the positive terminal of comparator 32].

With respect to claim 17, Schultz teaches that the comparator circuitry [Fig. 1, 32] is configured as a voltage comparator as disclosed in Fig. 1.

With respect to claim 19, it is well known in the art to use filters for smoothing signals before they are inputted into an internal circuitry].

With respect to claim 28, Schultz teaches that the second group of components includes a comparator [Fig. 1, 32], the comparator adapted to compare a first signal applied at the external connection with a second signal and provide an output dependent on that comparison.

4. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., in view of Ohnakado, Bradley and Schultz et al. as applied to claims 4-6, 8, 15-17, 19, and 28 above, and further in view of Hales, Patent No. 6,891,490. The prior art teaches a comparator circuitry but does not disclose that the comparator circuitry is configured as a SAR ADC or flash ADC. Hales teaches highly flexible devices used to convert an analog signal into a digital representation. With respect to claims 20 and 21, Hales teaches that it is well known that the comparator circuitry can be configured as a SAR ADC [Fig. 3, Col. 4, lines 47-52] or flash ADC [Fig. 4, Col. 5, lines 31-39]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hales, which teaches a SAR ADC and flash ADC, with

the comparator circuitry of Schultz for the benefit of noise reduction and the ability to use computers and computing software to analyze and manipulate the signal.

5. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., in view of Bradley, and further in view of Huang et al., Publication No. 2005/0224883.

Lee does not disclose that the first signal path includes up/down diode configuration adapted to provide protection from electrostatic discharge events. With respect to claim 23, Huang teaches an electrostatic discharge protection of semiconductor devices, the protection circuit comprises a first signal path that includes an up/down diode configuration [Fig. 1, 104, 106] adapted to provide protection from electrostatic discharge events [Paragraph 0016, lines 8-11].

Both teachings are analogous semiconductor devices having protective circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huang, which teaches an up/down diode configuration, with the semiconductor device of Lee for the benefit of protecting the internal circuitry from the ESD effects of the HBM and the MM by shorting the electrostatic pulses to either VCC or VSS.

With respect to claim 24, Huang teaches that the first signal path additionally includes an impedance element [Fig. 1, 108] in series with the up/down diode configuration [Fig. 1, Paragraph 0016, lines 12-13].

With respect to claim 25, Huang teaches that the first signal path additionally includes a digital buffer [Fig. 1, 118] in series with the up/down diode configuration [Fig. 1, Paragraph 0016, lines 17-20].

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Bradley, as applied to claim 26 above, and further in view of Ohnakado and Ker et al., Patent No. 6,750,517. Lee teaches a second signal path but does not disclose that the second signal path includes a MOS device with the source and well coupled together, the gate of the MOS device being controllable by a control voltage. Ohnakado teaches a second signal path that includes a MOS device [Fig. 2, 32] with the source and well coupled together.

Ker teaches an ESD protection circuit, the circuit comprises that the gate of the MOS device [Fig. 10, Mp, Col. 7, lines 48-50] is controllable by a control voltage, the MOS device being switchable between an off condition and an on condition, and wherein the off condition the MOS device presents a high impedance to the external connection.

All three teachings are analogous semiconductor devices having protective circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker, which teaches a gate of the MOS device being controllable by a control voltage, with the semiconductor device of Lee, modified by Ohnakado in order to control the voltage of a gate in a high voltage input condition.

Allowable Subject Matter

7. Claims 7, 9-11, 18, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 7: The prior art does not disclose that the amplifier is configured as an inverter. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 9: The prior teaches a second signal path but does not disclose that the second signal path is additionally coupled to an impedance device such that when the second signal path is operable, the pin sources current through the MOS device across the impedance, thereby causing the comparator circuitry to changes its output. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 18: The prior art teaches a MOS device and a comparator circuitry, but does not disclose that an analog filter is provided between the MOS device and the comparator circuitry. This feature in combination with the rest of the claims limitations is not anticipated or rendered obvious by the prior art of record.

The following is an examiner's statement of reasons for indicating allowance of claim 22: The prior art teaches a MOS device and a comparator, but does not disclose that the circuit further comprises at least one additional MOS device in the path between the first MOS device and the input to the comparator circuitry.

Response to Arguments

8. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 12, paragraph 3 and page 13 of the Remarks that the prior art does not disclose two signal paths on the same pad cell. Applicant argues that the two signal paths on the same pad cell is not the same as two signals paths on two different pad cells.

The new reference by Bradley [US Patent No. 6,550,664] teaches an integrated circuit, which teaches two signal paths [Fig. 4, 19 and 20] on the same pad cell [Fig. 12, Bonding pad].

Applicant argues on page 12, paragraph 4 of the Remarks that the prior art reduces capacitance and increases transmission speeds in the remainder of the circuit by blowing the fuse.

Lee [US Patent No. 6,329,563] teaches a pad cell that includes a first signal path being operational under a first set of normal operating conditions and a second signal path being non-operable under the first sent of normal operating

conditions, by blowing up the fuse. The Lee reference still reads on the claim language.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
10/13/2006

Stephen W Jackson
10-16-06

STEPHEN W. JACKSON
PRIMARY EXAMINER